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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,178	12/15/2004	Johannes Verhees	NL02 0513 US	5722

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EXAMINER

A, MINH D

ART UNIT PAPER NUMBER

2821

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No. 10/518,178	Applicant(s) VERHEES ET AL.	
	Examiner Minh D. A	Art Unit 2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/15/04.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/15/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-5 are rejected under 35 U.S.C. 102(a) as being anticipated by Ten Pierick et al (US 6,348,819).

Regarding claim 1, Ten Pierick et al discloses a control circuit(10) for controlling an electrical signal over a load(load circuit(4)) such as a deflection circuit of a Cathode Ray Tube, comprising a first transistor(switch) for switching the electrical signal over the load (4), wherein the load coupled to a collector and an emitter of the first transistor and wherein the control circuit(3) comprises a resonance circuit is coupled to a basis and the emitter f the first transistor for driving the first transistor, a power supply which is coupled to the resonance circuit for driving the resonance circuit , a pulse generating circuit which is coupled to the power supply and the resonance circuit , and a processing tunit with a memory unit characterised in that, the memory unit is arranged to be loaded with control information concerning predetermined states of the load and measurement circuit for corresponding predetermined optimal control adjustments of the power supply and/or the pulse generating circuit , wherein the processing unit is arranged for optimally controlling the electrical signal by controlling the first transistor via the power supply and/or via the pulse generating circuit

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for an actual state of the load on the basis of the control information loaded in the memory unit. See figures 1-4, col.2, lines 65-67 to col.6, lines 1-48.

Regarding claim 2, Ten Pierick et al discloses a control circuit for controlling an electrical signal over a load, the pulse generating circuit is arranged for generating a pulse signal for switching the first transistor via the resonance circuit . See figure 2.

Regarding claim 3, Ten Pierick et al discloses , the processing unit is coupled to the power supply for controlling the power supply. See figures 1-2.

Regarding claim 4, Ten Pierick et al discloses the control circuit for controlling the pulse generating circuit wherein the pulse generating circuit is arranged for pulse-width modulation of the pulse signal. See figures 1-4.

Regarding claim 5, Ten Pierick et al discloses the control circuit for controlling an electrical signal , the pulse generating circuit comprises a second transistor , a pulse generator which is coupled to a basis and an emitter of the second transistor and a transformer wherein a first coil f the transformer is coupled to the power supply and a collector of the second transistor and wherein a second coil of the transformer is coupled to the resonance circuit. See figure 2.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

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subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior art in view of Ten Pierick et al (US 6,348,819).

Regarding claims 6-7, Ten Pierick essentially discloses the claimed invention but does not explicitly disclose that the usages in LCR circuit or microprocessor and memory a digital EEPROM. It would have been an obvious matter of design choice to employ Ten Pierick in any desired interest environment in order to maximize the usage of his invention, since applicant does not disclose that, all of these limitations can solve any stated problem and for any particular purpose. Therefore, it appears that the invention would not provide any improvement but merely apply the invention in different presentation.

Allowable Subject Matter

5. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach that, the control circuit f having the steps of: coupling the basis and the emitter of the first transistor with factory measurement and control equipment; coupling the processing unit with factory measurement and control

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equipment; adjusting the load in an actual state of the load wherein the actual state of the load is one of the predetermined states of the load; adjusting the power supply (18) of the control circuit in a number of subsequent control adjustments of the power supply (18) for the actual state of the load with the factory measurement and control equipment, wherein the factory measurement and control equipment adjusts the processing unit, and wherein the processing unit controls the power supply in a number of control adjustments of the power supply ; measuring voltage response characteristics with the basis and the emitter of the first transistor (8) for each of the number of control adjustments of the power supply for the actual state of the load with the factory measurement and control equipment; selecting an optimal control adjustment from the number of control adjustments of the power supply for the actual state of the load on the basis of the measured voltage response characteristics with the factory measurement and control equipment; storing control information relating to the optimal control adjustment for the actual state of the load in the memory unit of the control circuit with the factory measurement and control equipment recited in dependent claim 8.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Hasegawa (US 6,046,623) and Suda et al (US 5,397,914) are cited to show a driving circuit for CRT.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Minh A whose telephone number is (571) 272-1817. The examiner can normally be reached on M-F (5:30 –2:30 PM).

If attempts to reach the examiner by telephone is unsuccessful, the examiner's supervisor, Don Wong, can be reached on (571) 272-1834. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and (703) 872-9319 for final communications.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (571) 272-1553.

Primary Examiner



Examiner

Minh A

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12/12/05